Patent
Attorney's Docket No. H1132

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	**Mail Stop: APPEAL BRIEF - PATENTS**
Ming-Ren LIN et al.	Group Art Unit: 2815
Application No.: 10/614,051	Examiner: P. Brock II
Filed: July 8, 2003	
For: METHOD FOR DOPING STRUCTURES IN FINFET DEVICES	

TRANSMITTAL FOR APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Appeal Brief-Patents
Randolph Building
401 Dulany Street
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Sir:

Transmitted herewith is an Appeal Brief in support of the Notice of Appeal filed March 25, 2005.

Enclosed is a check for ☐ $250.00 ☒ $500.00 to cover the Government fee.

The Commissioner is hereby authorized to charge any other appropriate fees that may be required by this paper that are not accounted for above, and to credit any overpayment, to Deposit Account No. 50-1070.

Respectfully submitted,

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Date: May 24, 2005

PATENT
Docket No. **H1132**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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APPEAL BRIEF

This Appeal Brief is submitted in response to the final Office Action, dated January 25, 2005, and in support of the Notice of Appeal, filed March 25, 2005.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Micro Devices, Inc.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

Appellants are unaware of any related appeals, interferences or judicial proceedings.

III. STATUS OF CLAIMS

Claims 1-20 are pending in this application.

Claims 1-20 were finally rejected in the Office Action, dated January 25, 2005, and are the subject of the present appeal. These claims are reproduced in the Claim Appendix of this Appeal Brief.

IV. STATUS OF AMENDMENTS

No amendments were filed subsequent to the final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In the paragraphs that follow, each of the independent claims and means plus function claims that is involved in this appeal and each dependent claim that is argued separately will be recited followed in parenthesis by examples of where support can be found in the specification and drawings.

Claim 1 recites a method for forming FinFET devices, comprising: forming a first fin structure (310, Fig. 3B), a source region (330, Fig. 3B), and a drain region (330, Fig. 3B) in a first area of a wafer (105, Fig. 1; pg. 4, para. 0019); forming a second fin structure (320, Fig. 3B), a source region (340, Fig. 3B), and a drain region (340, Fig. 3B) in a second area of the wafer (105, Fig. 1; pg. 4, para. 0019); forming a phosphosilicate glass layer on the first area and the second area (110, Fig. 1; 410, Fig. 4; pg. 4, para. 0020); removing the phosphosilicate glass layer from the second area (115, Fig. 1; pg. 5, para. 0021); forming a boron silicate glass layer on the first area and the second area (120, Fig. 1; 610, Fig. 6; pg. 5, para. 0022); annealing the first area

and the second area, the annealing causing the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causing the second fin structure, source region, and drain region of the second area to be doped with boron (125, Fig. 1; pg. 5, para. 0023); removing the boron silicate glass layer from the first area and the second area (130, Fig. 1; pg. 5, para. 0023); and removing the phosphosilicate glass layer from the first area (130, Fig. 1; pg. 5, para. 0023).

Claim 7 recites a method for doping a fin structure and source and drain regions in FinFET devices, comprising: forming a first glass layer (410, Fig. 4) on the fin structure (310, 320, Fig. 3B) and source and drain regions (330, 340, Fig. 3B) of an N-channel device and a P-channel device (110, Fig. 1; pg. 4, para. 0020); removing the first glass layer from the P-channel device (115, Fig. 1; pg. 5, para. 0021); forming a second glass layer (610, Fig. 6) on the fin structure (310, 320, Fig. 3B) and source and drain regions (330, 340, Fig. 3B) of the N-channel device and the P-channel device, the second glass layer being different than the first glass layer (120, Fig. 1; pg. 5, para. 0022); and annealing the N-channel device and the P-channel device to dope the fin structure and source and drain regions of the N-channel device and the P-channel device (125, Fig. 1; pg. 5, para. 0023).

Claim 13 recites a method for doping fin structures in FinFET devices, comprising: forming a first glass layer (410, Fig. 4) on the fin structures (310, 320, Fig. 3B) of a first area and a second area (110, Fig. 1; pg. 4, para. 0020); removing the first glass layer from the second area (115, Fig. 1; pg. 5, para. 0021); forming a second glass layer (610, Fig. 6) on the fin structures (310, 320, Fig. 3B) of the first area and the second area (120, Fig. 1; pg. 5, para. 0022); and annealing the first area and the second area to dope the fin structures of the first area and the

second area (125, Fig. 1; pg. 5, para. 0023).

Claim 20 recites that the forming a first glass layer includes forming the first glass layer directly on the fin structures of the first area and the second area (410, Fig. 4).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 13, 14, and 20 stand rejected under 35 U.S.C. § 102(e) as anticipated by Wu et al. (U.S. Patent Application Pub. No. 2004/0048424).

B. Claims 1-12 and 15-19 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Wu et al. (U.S. Patent Application Pub. No. 2004/0048424) in view of Frenette et al. (U.S. Patent No. 5,770,490).

VII. ARGUMENT

A. Rejection under 35 U.S.C. § 102(e) based on Wu et al. (U.S. Patent Application Pub. No. 2004/0048424).

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention always rests upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987).

1. Claims 13 and 14.

With the above principles in mind, Appellants' claim 13 is directed to a method for

doping fin structures in FinFET devices. The method includes forming a first glass layer on the fin structures of a first area and a second area; removing the first glass layer from the second area; forming a second glass layer on the fin structures of the first area and the second area; and annealing the first area and the second area to dope the fin structures of the first area and the second area. Wu et al. does not disclose or suggest this combination of features.

For example, Wu et al. does not disclose or suggest annealing a first area and a second area to dope the fin structures of the first area and the second area. The Examiner relies on Fig. 9B and para. 0023 of Wu et al. for allegedly disclosing this feature (final Office Action, pg. 2). Appellants disagree.

Fig. 9B of Wu et al. depicts a cross-sectional view of a FinFET device where the portion of the FinFET under PSG layer 12 is an N type source/drain region 40 and the portion of the FinFET under BSG layer 10 is a P type source/drain region 30. This figure of Wu et al. in no way discloses or suggests annealing the first area and the second area to dope the fin structures of the first area and the second area, as required by claim 13. Contrary to the Examiner's position, Fig. 9B of Wu et al. does not disclose fin structures, but merely an N type source/drain region 40 and a P type source/drain region 30. As will be appreciated by one skilled in the art, a fin structure for a FinFET device is positioned between the source and drain regions of the FinFET device. Therefore, as illustrated in Wu et al.'s Fig. 9A, the fin structures of Wu et al.'s FinFET device are positioned below gate structure 8. Wu et al. does not disclose or suggest annealing the first area and the second area to dope the fin structures of the first area and the second area, as required by claim 13.

At para. 0023, Wu et al. discloses:

> An anneal procedure is next performed at a temperature between about 700 to 1000 °C, for a time between about 1 to 60 min, in a conventional furnace, or via use of rapid thermal anneal (RTA) procedures. The anneal procedure allows the doping of the exposed SOI shapes which directly underlay the doped insulator layer, resulting in doped source/drain regions. The portion of FINFET shape 5, underlying PSG layer 12, is now N type source/drain region 40, while the portions of FINFET shape 6, underlying BSG layer 10, is now P type source/drain region 30. This is schematically shown in cross-sectional style in FIG. 9B, and as a top view using FIG. 9A. Therefore a desired NMOS FINFET device, featuring N type source/drain region 40, and a desired PMOS FINFET device, featuring P type source/drain region 30, is defined in the same SOI layer.

This section of Wu et al. discloses annealing the FinFET device to dope the source and drain regions. This section of Wu et al. in no way discloses or suggests annealing a first area and a second area to dope the fin structures of the first area and the second area, as required by claim 13. Instead, as set forth above, Wu et al. merely discloses the doping of source and drain regions.

In the final Office Action, the Examiner alleges, in response to the above arguments, that "it is not clear why portions 30 and 40 are not considered fin structures" (final Office Action, pp. 9-10). As set forth above, one skilled in the art would readily appreciate that a fin structure for a FinFET device is positioned between the source and drain regions of the FinFET device. This well-known definition of a fin structure for a FinFET device is depicted, for example, in Appellants' Fig. 3B. Wu et al.'s source and drain regions 30 and 40 are not fin structures, as the phrase "fin structure" is known in the art.

Wu et al. specifically discloses that the anneal procedure allows doping of the exposed silicon-on-insulator (SOI) shapes which directly underlay the doped insulator layer to produce source/drain regions 30 and 40 (para. 0023). Wu et al. does not disclose or suggest that the fin structures located between these source/drain regions 30 and 40 are doped, as required by claim 13. More particularly and as set forth above, Wu et al. does not disclose or suggest that the fin

structure located below gate 8 is doped as a result of the anneal procedure. Therefore, Wu et al. cannot disclose or suggest annealing the first area and the second area to dope the fin structures of the first area and the second area, as required by claim 13.

Further with respect to the above feature of claim 13, the Examiner alleges "it is noted that the features upon which applicant relies (i.e., 'a fin structure of a FINFET device is positioned between the source and drain regions of the FINFET device') are not recited in the rejected claim(s)" (final Office Action, pg. 10). Appellants disagree.

As noted above, one skilled in the art would readily appreciate that a fin structure for a FinFET device is positioned between the source and drain regions of the FinFET device. Moreover, even assuming, for the sake of argument that fin structures are defined in some other way, it has been repeatedly held that where an explicit definition is provided by Appellants for a term, that definition will control interpretation of the term as it is used in the claim. See, for example, Toro Co. v. White Consolidated Industries Inc., 199 F.3d 1295, 1301, 53 USPQ2d 1065, 1069 (Fed. Cir. 1999). As clearly supported by Appellants' specification, the fin structure is a structure that is positioned between the source and drain regions of the FinFET device (see, for example, elements 310 and 320 in Fig. 3B).

Since Wu et al. does not disclose every feature of Appellants' claim 13, Wu et al. does not anticipate claim 13.

For at least the foregoing reasons, Appellants submit that the rejection of claim 13 under 35 U.S.C. § 102(e) based on Wu et al. is improper. Accordingly, Appellants request that the rejection be reversed.

2. Claim 20.

Claim 20 depends from claim 13. Therefore, claim 20 is not anticipated by Wu et al. for at least the reasons given above with respect to claim 13. Moreover, claim 20 recites an additional feature that is not disclosed or suggested by Wu et al.

Claim 20 recites that the forming a first glass layer includes forming the first glass layer directly on the fin structures of the first area and the second area. The Examiner relies on Fig. 7b and para. 0021 of Wu et al. for allegedly disclosing this feature (final Office Action, pg. 3). Appellants submit that these sections of Wu et al. do not disclose or suggest forming the first glass layer directly on the fin structures of the first area and the second area, as required by claim 20.

Fig. 7b of Wu et al. depicts a borosilicate glass (BSG) layer 10 being formed over a PMOS FinFET device region. As is more clearly illustrated in Fig. 7a of Wu et al., BSG layer 10 is not formed directly on the fin structure that is located below gate structure 8. Therefore, these figures of Wu et al. do not disclose or suggest forming the first glass layer directly on the fin structures of the first area and the second area, as required by claim 20.

At para. 0021, Wu et al. discloses:

> A borosilicate glass (BSG), layer 10, is next deposited at a thickness between about 100 to 2000 Angstroms, via PECVD or LPCVD procedures. The weight percent of B_2O_3 in BSG layer 10, is between about 3 to 10%. Photoresist shape 11, schematically shown in cross-sectional style in FIG. 7B, is used as a mask to allow removal of a portion of BSG layer 10, in a region to be used to accommodate a subsequent NMOS FINFET device, to be accomplished. Removal of the exposed portion of BSG layer 10, is achieved via a RIE procedure using CHF_3 as an etchant, or via a wet etch procedure using a buffered hydrofluoric (BHF) acid solution as an etchant. A top view showing BSG layer only overlying a subsequent PMOS FINFET device region, is schematically shown in FIG. 7A.

This section of Wu et al. discloses forming BSG layer 10 over a PMOS FinFET device region.

This section of Wu et al. does not disclose or suggest forming the first glass layer directly on the fin structures of the first area and the second area, as required by claim 20.

For at least the foregoing reasons, Appellants submit that the rejection of claim 20 under 35 U.S.C. § 102(e) based on Wu et al. is improper. Accordingly, Appellants request that the rejection be reversed.

B. Rejection under 35 U.S.C. § 103(a) based on Wu et al. (U.S. Patent Application Pub. No. 2004/0048424) in view of Frenette et al. (U.S. Patent No. 5,770,490).

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention always rests upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In rejecting a claim under 35 U.S.C. § 103, the Examiner must provide a factual basis to support the conclusion of obviousness. In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). Based upon the objective evidence of record, the Examiner is required to make the factual inquiries mandated by Graham v. John Deere Co., 86 S.Ct. 684, 383 U.S. 1, 148 USPQ 459 (1966). The Examiner is also required to explain how and why one having ordinary skill in the art would have been realistically motivated to modify an applied reference and/or combine applied references to arrive at the claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

In establishing the requisite motivation, it has been consistently held that the requisite motivation to support the conclusion of obviousness is not an abstract concept, but must stem from the prior art as a whole to impel one having ordinary skill in the art to modify a reference or

to combine references with a reasonable expectation of successfully achieving some particular realistic objective. See, for example, Interconnect Planning Corp. v. Feil, 227 USPQ 543 (Fed. Cir. 1985). Consistent legal precedent admonishes against the indiscriminate combination of prior art references. Carella v. Starlight Archery, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985).

1. Claims 1-6.

Independent claim 1 is directed to a method for forming FinFET devices. The method includes forming a first fin structure, a source region, and a drain region in a first area of a wafer; forming a second fin structure, a source region, and a drain region in a second area of the wafer; forming a phosphosilicate glass layer on the first area and the second area; removing the phosphosilicate glass layer from the second area; forming a boron silicate glass layer on the first area and the second area; annealing the first area and the second area, where the annealing causes the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causes the second fin structure, source region, and drain region of the second area to be doped with boron; removing the boron silicate glass layer from the first area and the second area; and removing the phosphosilicate glass layer from the first area. Wu et al. and Frenette et al. do not disclose or suggest this combination of features.

For example, Wu et al. and Frenette et al. do not disclose or suggest annealing the first area and the second area, where the annealing causes the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causes the second fin structure, source region, and drain region of the second area to be doped with boron. The Examiner relies

on Fig. 9B and para. 0023 of Wu et al. for allegedly disclosing this feature (final Office Action, pg. 4). Appellants disagree.

Fig. 9B of Wu et al. depicts a cross-sectional view of a FinFET device where the portion of the FinFET under PSG layer 12 is an N type source/drain region 40 and the portion of the FinFET under BSG layer 10 is a P type source/drain region 30. This figure of Wu et al. in no way discloses or suggests annealing the first area and the second area, where the annealing causes the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causes the second fin structure, source region, and drain region of the second area to be doped with boron, as required by claim 1. Contrary to the Examiner's position, Fig. 9B of Wu et al. does not disclose fin structures, but merely an N type source/drain region 40 and a P type source/drain region 30. As discussed previously with respect to claim 13 and as will be appreciated by one skilled in the art, a fin structure for a FinFET device is positioned between the source and drain regions of the FinFET device. Therefore, as illustrated in Wu et al.'s Fig. 9A, the fin structures of Wu et al.'s FinFET device are positioned below gate structure 8. Wu et al. does not disclose or suggest annealing the first area and the second area, where the annealing causes the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causes the second fin structure, source region, and drain region of the second area to be doped with boron, as required by claim 1.

At para. 0023, Wu et al. discloses:

> An anneal procedure is next performed at a temperature between about 700 to 1000 °C, for a time between about 1 to 60 min, in a conventional furnace, or via use of rapid thermal anneal (RTA) procedures. The anneal procedure allows the doping of the exposed SOI shapes which directly underlay the doped insulator layer, resulting in doped source/drain regions. The portion of FINFET shape 5,

> underlying PSG layer 12, is now N type source/drain region 40, while the portions of FINFET shape 6, underlying BSG layer 10, is now P type source/drain region 30. This is schematically shown in cross-sectional style in FIG. 9B, and as a top view using FIG. 9A. Therefore a desired NMOS FINFET device, featuring N type source/drain region 40, and a desired PMOS FINFET device, featuring P type source/drain region 30, is defined in the same SOI layer.

This section of Wu et al. discloses annealing the FinFET device to dope the source and drain regions. This section of Wu et al. in no way discloses or suggests annealing the first area and the second area, where the annealing causes the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causes the second fin structure, source region, and drain region of the second area to be doped with boron, as required by claim 1. Instead, as set forth above, Wu et al. merely discloses the doping of source and drain regions. The disclosure of Frenette et al. does not remedy this deficiency in the disclosure of Wu et al.

In response to the above arguments, the Examiner alleges that "it should be noted that the first and second fin structures consist of their respective source regions and drain regions. Thus, since the source regions and drain regions of the first and second fin structures, in the first and second areas, are doped in the annealing step described in figure 9B and paragraph 0023, it can further be acknowledged that the first and second fin structures are themselves doped" (final Office Action, pg. 11). Appellants disagree.

Claim 1 specifically recites a first fin structure, a source region, and a drain region in a first area of a wafer and a second fin structure, a source region, and a drain region in a second area of the wafer. It is unclear how the Examiner can reasonably allege that the first fin structure in the first area is the same as the source region and drain region in the first area when claim 1 specifically recites three separate elements in the first area. Moreover, it is unclear how the

Examiner can reasonably allege that the second fin structure in the second area is the same as the source region and drain region in the second area when claim 1 specifically recites three separate elements in the second area. The Examiner has not logically explained how Wu et al.'s source/drain regions 30 and 40 can reasonably be construed as a source region, a drain region, and a fin structure.

Nevertheless, as set forth above, one skilled in the art would readily appreciate that a fin structure for a FinFET device is positioned between the source and drain regions of the FinFET device. Moreover, even assuming, for the sake of argument that fin structures are defined in some other way, it has been repeatedly held that where an explicit definition is provided by Appellants for a term, that definition will control interpretation of the term as it is used in the claim. See, for example, Toro Co. at 1301. As clearly supported by Appellants' specification, the fin structure is positioned between the source and drain regions of the FinFET device (see, for example, elements 310 and 320 in Fig. 3B). Therefore, it is clear that the recited first and second fin structures are not source/drain regions, as the Examiner alleges.

The Examiner has not pointed to any section of Wu et al. or Frenette et al. that discloses or suggests annealing a first area and a second area, where the annealing causes the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causes the second fin structure, source region, and drain region of the second area to be doped with boron, as required by claim 1.

For at least the foregoing reasons, Appellants submit that the rejection of claim 1 under 35 U.S.C. § 103(a) based on Wu et al. and Frenette et al. is improper. Accordingly, Appellants request that the rejection be reversed.

2. Claims 7-12.

Independent claim 7 is directed to a method for doping a fin structure and source and drain regions in FinFET devices. The method includes forming a first glass layer on the fin structure and source and drain regions of an N-channel device and a P-channel device; removing the first glass layer from the P-channel device; forming a second glass layer on the fin structure and source and drain regions of the N-channel device and the P-channel device, the second glass layer being different than the first glass layer; and annealing the N-channel device and the P-channel device to dope the fin structure and source and drain regions of the N-channel device and the P-channel device. Wu et al. and Frenette et al. do not disclose or suggest this combination of features.

For example, Wu et al. and Frenette et al. do not disclose or suggest annealing the N-channel device and the P-channel device to dope the fin structure and source and drain regions of the N-channel device and the P-channel device. The Examiner relies on Fig. 9B and para. 0023 of Wu et al. for allegedly disclosing this feature (final Office Action, pg. 7). Appellants disagree.

As discussed above with respect to claim 1, Fig. 9B of Wu et al. depicts a cross-sectional view of a FinFET device where the portion of the FinFET under PSG layer 12 is an N type source/drain region 40 and the portion of the FinFET under BSG layer 10 is a P type source/drain region 30. This figure of Wu et al. in no way discloses or suggests annealing the N-channel device and the P-channel device to dope the fin structure and source and drain regions of the N-channel device and the P-channel device, as required by claim 7. Contrary to the Examiner's position, Fig. 9B of Wu et al. does not disclose fin structures, but merely an N type source/drain

region 40 and a P type source/drain region 30. As will be appreciated by one skilled in the art, a fin structure for a FinFET device is positioned between the source and drain regions of the FinFET device. Therefore, as illustrated in Wu et al.'s Fig. 9A, the fin structures of Wu et al.'s FinFET device are positioned below gate structure 8. Wu et al. does not disclose or suggest annealing the N-channel device and the P-channel device to dope the fin structure and source and drain regions of the N-channel device and the P-channel device, as required by claim 7.

At para. 0023, Wu et al. discloses:

> An anneal procedure is next performed at a temperature between about 700 to 1000 °C, for a time between about 1 to 60 min, in a conventional furnace, or via use of rapid thermal anneal (RTA) procedures. The anneal procedure allows the doping of the exposed SOI shapes which directly underlay the doped insulator layer, resulting in doped source/drain regions. The portion of FINFET shape 5, underlying PSG layer 12, is now N type source/drain region 40, while the portions of FINFET shape 6, underlying BSG layer 10, is now P type source/drain region 30. This is schematically shown in cross-sectional style in FIG. 9B, and as a top view using FIG. 9A. Therefore a desired NMOS FINFET device, featuring N type source/drain region 40, and a desired PMOS FINFET device, featuring P type source/drain region 30, is defined in the same SOI layer.

This section of Wu et al. discloses annealing the FinFET device to dope the source and drain regions. This section of Wu et al. in no way discloses or suggests annealing the N-channel device and the P-channel device to dope the fin structure and source and drain regions of the N-channel device and the P-channel device, as required by claim 7. Instead, as set forth above, Wu et al. merely discloses the doping of source and drain regions. The disclosure of Frenette et al. does not remedy this deficiency in the disclosure of Wu et al.

The Examiner alleges that "it should be noted that the first and second fin structures consist of their respective source regions and drain regions. Thus, since the source regions and drain regions of the first and second fin structures, in the first and second areas, are doped in the

annealing step described in figure 9B and paragraph 0023, it can further be acknowledged that the first and second fin structures are themselves doped" (final Office Action, pg. 11). Appellants disagree.

Claim 7 specifically recites a fin structure, a source region, and a drain region. It is unclear how the Examiner can reasonably allege that the fin structure is the same as the source region and drain region when claim 7 specifically recites three separate elements. The Examiner has not logically explained how Wu et al.'s source/drain regions 30 and 40 can reasonably be construed as a source region, a drain region, and a fin structure.

Nevertheless, as set forth above, one skilled in the art would readily appreciate that a fin structure for a FinFET device is positioned between the source and drain regions of the FinFET device. Moreover, even assuming, for the sake of argument that fin structures are defined in some other way, it has been repeatedly held that where an explicit definition is provided by Appellants for a term, that definition will control interpretation of the term as it is used in the claim. See, for example, Id. As clearly supported by Appellants' specification, the fin structure is a structure that is positioned between the source and drain regions of the FinFET device (see, for example, Fig. 3B). Therefore, it is clear that the recited fin structure is not a source/drain region, as the Examiner alleges.

The Examiner has not pointed to any section of Wu et al. or Frenette et al. that discloses or suggests annealing the N-channel device and the P-channel device to dope the fin structure and source and drain regions of the N-channel device and the P-channel device, as required by claim 7.

For at least the foregoing reasons, Appellants submit that the rejection of claim 7 under 35 U.S.C. § 103(a) based on Wu et al. and Frenette et al. is improper. Accordingly, Appellants request that the rejection be reversed.

3. Claims 15-19.

Claims 15-19 depend from claim 13. The disclosure of Frenette et al. does not remedy the deficiencies in the disclosure of Wu et al. set forth above with respect to claim 13. Therefore, claim 13 is patentable over Wu et al. and Frenette et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 13.

VIII. CONCLUSION

In view of the foregoing arguments, Appellants respectfully solicit the Honorable Board to reverse the Examiner's rejections of claims 1-20 under 35 U.S.C. §§ 102 and 103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

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IX. CLAIM APPENDIX

1. A method for forming FinFET devices, comprising:

forming a first fin structure, a source region, and a drain region in a first area of a wafer;

forming a second fin structure, a source region, and a drain region in a second area of the wafer;

forming a phosphosilicate glass layer on the first area and the second area;

removing the phosphosilicate glass layer from the second area;

forming a boron silicate glass layer on the first area and the second area;

annealing the first area and the second area, the annealing causing the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causing the second fin structure, source region, and drain region of the second area to be doped with boron;

removing the boron silicate glass layer from the first area and the second area; and

removing the phosphosilicate glass layer from the first area.

2. The method of claim 1 wherein the forming a phosphosilicate glass layer on the first area and the second area includes:

depositing phosphosilicate glass to a thickness ranging from about 100 Å to about 500 Å.

3. The method of claim 1 wherein the forming a boron silicate glass layer on the first

area and the second area includes:

depositing boron silicate glass to a thickness ranging from about 100 Å to about 500 Å.

4. The method of claim 1 wherein the first area is an N-channel area.

5. The method of claim 4 wherein the second area is a P-channel area.

6. The method of claim 1 wherein the removing a phosphosilicate glass layer from the second area includes:

masking the first area, and

etching the phosphosilicate glass from the second area.

7. A method for doping a fin structure and source and drain regions in FinFET devices, comprising:

forming a first glass layer on the fin structure and source and drain regions of an N-channel device and a P-channel device;

removing the first glass layer from the P-channel device;

forming a second glass layer on the fin structure and source and drain regions of the N-channel device and the P-channel device, the second glass layer being different than the first glass layer; and

annealing the N-channel device and the P-channel device to dope the fin structure

and source and drain regions of the N-channel device and the P-channel device.

8. The method of claim 7 further comprising:

removing the second glass layer from the N-channel device and the P-channel device; and

removing the first glass layer from the N-channel device.

9. The method of claim 7 wherein the first glass layer comprises phosphosilicate glass and the second glass layer comprises boron silicate glass.

10. The method of claim 9 wherein the forming a first glass layer on the N-channel device and the P-channel device includes:

depositing phosphosilicate glass to a thickness ranging from about 100 Å to about 500 Å.

11. The method of claim 10 wherein the forming a second glass layer on the N-channel device and the P-channel device includes:

depositing boron silicate glass to a thickness ranging from about 100 Å to about 500 Å.

12. The method of claim 7 wherein the removing the first glass layer from the P-channel device includes:

forming a mask on the N-channel device, and

etching the first glass layer from the P-channel device.

13. A method for doping fin structures in FinFET devices, comprising:

forming a first glass layer on the fin structures of a first area and a second area;

removing the first glass layer from the second area;

forming a second glass layer on the fin structures of the first area and the second area; and

annealing the first area and the second area to dope the fin structures of the first area and the second area.

14. The method of claim 13 further comprising:

removing the second glass layer from the first area and the second area; and

removing the first glass layer from the first area.

15. The method of claim 13 wherein the first glass layer comprises phosphosilicate glass and the second glass layer comprises boron silicate glass.

16. The method of claim 15 wherein the first area is an N-channel area and the second area is a P-channel area.

17. The method of claim 13 wherein the forming a first glass layer includes:

depositing phosphosilicate glass to a thickness ranging from about 100 Å to about 500 Å.

18. The method of claim 17 wherein the forming a second glass layer includes:

depositing boron silicate glass to a thickness ranging from about 100 Å to about 500 Å.

19. The method of claim 13 wherein the annealing causes the fin structure in the first area to be doped with phosphorus and the fin structure in the second area to be doped with boron.

20. The method of claim 13 wherein the forming a first glass layer includes:

forming the first glass layer directly on the fin structures of the first area and the second area.